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PLL WITH MEMORY FOR ELECTRONIC ALIGNMENTS

Field of the Invention

The invention generally relates to television receivers, and more particularly, to tuners used in televisions.

Description of the Background Art

Television tuners are usually implemented in television devices (such as television receivers, VCR's, etc.) either as discrete tuner modules or as on-board tuner circuits on digital decoder unit chassis ("tuner-on-board"). Both discrete tuner modules and on-board tuner circuits often include phase-locked loop (PLL) circuits.

FIG. 1 shows one embodiment of a television control system 100 to be used in a television receiver. The television control system includes a microprocessor 102, a chassis nonvolatile memory 104, a communication bus 106, a tuner module 108 such as a single-conversion tuner, and an RF source 110 such as an antenna or cable wire. The tuner module 108 comprises a PLL integrated circuit 112 of the tuner module. The communication bus 106 electronically connects the microprocessor 102 to the PLL integrated circuit 112. The microprocessor 102 is electrically connected to the chassis nonvolatile memory 104.

The manufacture of tuners for television receivers includes an alignment process for adjusting the tuners to perform fairly equal over the entire frequency band of operation. Presently, there are two general methods for aligning a television tuner: mechanical alignment and electronic alignment. Mechanical alignment involves slight changes in the location of sensitive components in the tuner (e.g. coils and the like) that maximize the performance of the tuner. Mechanical alignment is generally accomplished via human interaction at the end of the production line, and as such is generally inefficient.

Electronic alignment is a process whereby alignment data for a particular tuner is stored in non-volatile memory contained in the television receiver. When the user selects a desired channel, a microprocessor within the television receiver looks up the alignment data stored in the non-volatile memory for the desired channel and communicates this alignment data to the television tuner. The tuner then compensates for mismatches and keeps tuning performance constant. The D/A converter circuits are provided in the tuners to electronically "align" the tuners to provide optimum frequency adjustment (i.e. "trimming") of the tuners

by converting the digitally stored alignment data to analog voltages that align circuits.

While electronic alignment reduces human interaction on the production line, it narrows compatibility among the television receiver components. The microprocessor must contain specific routines for selecting and communicating the alignment data from the non-volatile memory to the tuner. The tuner must be adapted to accept the data and compensate for mismatches. As such, replacement of a malfunctioning television tuner in the field requires finding a new television tuner that is adapted to the specific television control system.

When a discrete tuner module (not a tuner-on-board type tuner) is utilized, different data must be provided for the chassis nonvolatile memory, depending upon the specific characteristics of tuner module to be used with a particular chassis. For example, a tuner used in Europe uses different alignment data than a tuner used in the United States. Such alignment data is stored in the chassis nonvolatile memory that interacts with the microprocessor to retrieve the alignment data since the unique alignment data is stored in the discrete tuner modules. Not only is the alignment data for tuners used in different regions in the world different, but alignment data used in each tuner is typically unique. The reasons why each tune contain different alignment data includes layout differences and component tolerance variations. The layout differences in the alignment data compensate for particularities of the printed circuit board for each television set. The component tolerance variations in the alignment data compensate for component value variations. Storing various alignment data in the chassis nonvolatile memory for each tuner is time consuming and complicates the manufacturing processes.

The tuner 108 of the television control system 100 shown in Fig. 1 that utilizes electronic alignment data is input into the television receiver at the time of manufacture. However, alignment data used for the tuner functions are stored in the chassis nonvolatile memory 104 and retrieved by the microprocessor 102. As such, the microprocessor 102 has to perform the functions associated with the retrieval of the alignment data. During manufacture of the television set, the different components are assembled.

The alignment data is not stored in the tuner, but is instead contained in the chassis nonvolatile memory 104 at the time of component assembly. The alignment data that pertains to a particular tuner is separately programmed into the chassis nonvolatile memory during component assembly. As such, each tuner that is shipped from the location of tuner manufacture to the location of component assembly has to contain the tuner in addition to alignment data that

is a separate entity from the tuner. During assembly, not only is the tuner installed into the television, but the alignment data has to be correctly stored into the chassis nonvolatile memory. If the alignment data is incorrectly entered into the chassis nonvolatile memory, then the tuner will not function properly.

If a television receiver is not tuning properly, either the tuner module 108 is defective or the alignment data transmitted to the tuner 108 from the microprocessor is defective. A repair person fixing such a tuning malfunction could not be certain that replacing the tuner module 108 itself would correct the tuner deficiency because the malfunction in the alignment data could originate in the microprocessor, the chassis nonvolatile memory 104, or the tuner itself.

Therefore, a need exists in the art for a tuner having a non-volatile memory that contains its own alignment data.

SUMMARY OF THE INVENTION

The present invention relates to tuner devices. More particularly, a tuner comprises a phase-locked loop circuit, D/A converter circuits, and a non-volatile memory. The disadvantages associated with the prior art are overcome by a television control system that exhibits modular tuner compatibility. Specifically, electronic alignment data for a tuner module of a television receiver is stored in non-volatile memory that is located within the tuner module. The microprocessor within the television receiver communicates a tuning command to the tuner module that contains the desired television channel. The tuner module accesses the non-volatile memory for the alignment data corresponding with the desired television channel and performs the alignment.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1A shows a block diagram of one embodiment of a television receiver including a tuner;

FIG. 1 shown a block diagram of one embodiment of tuner;

FIG. 2 shows a block diagram of another embodiment of tuner;

FIG. 2A depicts a block diagram of a television receiver having a television control system of the present invention.

FIG. 3 shows a block diagram of one embodiment of PLL circuit;

FIG. 4 shows a block diagram of another embodiment of PLL circuit; and

FIG. 5 discloses one embodiment of software for an address decoder;

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION

After considering the following description, those skilled in the art will clearly realize that the teachings of this invention can be readily utilized in television receivers. This disclosure involves a television tuner in which a re-writable memory is associated with a PLL integrated circuit to store alignment data within the tuner.

FIG. 1A shows one embodiment of a television receiver 150. The television receiver 150 includes a television control system 100, a radio frequency (RF) source 110, and a screen 156. The television control system 100 includes a tuner module 108 and a microprocessor 102. Received television signals from an RF source 110, a cable, a digital video disk device, a VCR, a computer, or any known device by which televisions receive signals are displayed on the television screen 156.

The tuner module 108 selects the RF signal corresponding to a desired television channel selected from a plurality of channel locations in a frequency band provided by the RF source 110 (e.g., antenna, cable feed, or the like). The RF signals associated with television channels are analog and digital television signals. The analog television signal may comprise a conventional National Television Standard Committee (NTSC) modulated signal within the United States. The digital television signal may comprise a Vestigial Sideband (VSB) modulated signal in compliance with the Advanced Television Systems Committee (ATSC) standard A/53, for example, a high definition television (HDTV) signal. The system described herein could also be configured to function with other formats, such as European, by appropriate changes in the television control system 100.

The tuner module 108 selects the desired television channel to be displayed on the screen 156 pursuant to a tuning command generated by the microprocessor 102. The microprocessor 102 is coupled to the tuner module 108 via the communication bus 106. In this disclosure, the communication bus may be an inter-integrated circuit (I2C) bus, a 3-wire bus, or any known type of communication bus. In response to the tuning command generated by the microprocessor 102, the tuner module 108 searches the memory unit 203 for the alignment data corresponding with the desired television channel. The memory unit 203 comprises nonvolatile memory. In this disclosure, nonvolatile memory may include, but is not limited to, read only memory (ROM) or

programmable ROM (PROM), the latter of which may be subdivided into electrically programmable ROM (EPROM), electrically erasable programmable ROM (EEPROM), and one-time PROM (OTPROM). The alignment data comprises data necessary to compensate for mismatches in the preset alignment of various sensitive components within the tuner module 108, such as tuning coils.

In this manner, the tuner module 108 is electronically aligned to provide the best overall tuning performance for the desired television channel. The tuner module 108 contains all the necessary data for tuner alignment thus dispensing with the need to embed tuner specific routines for selecting and communicating alignment data from the microprocessor 102 to the tuner module 108. As such, the tuner module 108 is a discrete component within the television control system 100, which allows, for example, the replacement of the tuner module 108 in the field without changing the television control system 100, specifically, the microprocessor 102.

In the embodiment of television control system 100 shown in Fig. 2, a re-writable memory, e.g. PLL nonvolatile memory 203, is located internal to the tuner module 108 and is electrically connected to the PLL integrated circuit 112. The PLL nonvolatile memory 203 stores alignment data and can store additional data relating to the operation of the PLL nonvolatile memory. By storing the alignment data in the PLL nonvolatile memory in the tuner module 108, the alignment data can be selected depending upon the specifics of the tuner to be used in the television control system 100. Variations in the alignment data between different tuners can result from layout differences that reflect printed circuit board distinctions, component tolerances that reflect component value variations, and the broadcast characteristics in the region of the world that the tuner is being used. Each tuner contains specific alignment data. The alignment data is entered into a discrete tuner module 108 at time of manufacture by the manufacturer, distributor, or other person. The alignment data remains with the tuner module 108, and can be transferred between different television sets by transfer of the tuner module.

The PLL 112 utilizes a PLL oscillator 208 and a reference oscillator (not shown). The PLL oscillator 208 can be controlled to operate over the desired frequency range of the PLL integrated circuit. The reference oscillator is, e.g., a crystal oscillator that is used to steer the PLL frequency generated by the PLL oscillator. During operation, the frequency of the PLL oscillator 208 is compared to the frequency of the reference oscillator. If a comparator circuit notes that the PLL signal is leading the signal generated by the reference oscillator, the frequency of the PLL signal generated by the PLL oscillator 208 is decreased. If

the comparator circuit notes that the PLL signal is lagging the signal generated by the reference oscillator, the frequency of the PLL signal generated by the PLL oscillator 208 is increased. The PLL circuits can be combined with the local oscillator, mixer circuits, and a D/A converter into a single tuner integrated circuit. Also, a similar PLL circuit that includes nonvolatile memory storage can be used in a double-conversion tuner architecture, with memory included in either or both PLL circuits. One system that utilizes a phase-locked loop is disclosed in U.S. Patent 5,828,266, issued October 28, 1998 to Couet, entitled "APPARATUS AND METHODS FOR SETTING UP A TUNING FREQUENCY OF A PLL DEMODULATOR THAT COMPENSATES FOR DISPERSION AND AGING EFFECTS OF AN ASSOCIATED CERAMIC RESONATOR FREQUENCY REFERENCE" (incorporated herein by reference).

The tuning algorithm can be simplified because the alignment data in the tuner is recalled in response to the frequency programmed in the PLL nonvolatile memory 203. In addition, microprocessor intervention for alignments will not be necessary once values are stored in the PLL nonvolatile memory. The cost and space requirements of providing a separate memory device, and its associated interface circuitry, when the television control system 100 is used in a different location (country, etc.) or with a different tuner to cause the alignment data in the EEPROM 104 to correspond to the tuner specifics can be limited.

FIG. 2A depicts a block diagram of another embodiment of television receiver 150 incorporating the television control system 100 of the present invention. The television receiver 150 comprises a tuner module 108, a microprocessor 102, an RF source 110, an IF module 212, and a demodulation module 214. The tuner module 108 selects the RF signal corresponding with the desired television channel from the RF source 110. The desired television channel is communicated to the microprocessor 102 via user input. The microprocessor 102 sends a tuner command signal over the communication bus to the tuner module 108. The tuner module 108 performs electronic alignment and couples the RF signal corresponding with the desired television channel to the IF module 212. The IF module 212 and the demodulation module 214, in a well known manner, convert the RF signal to an IF signal and demodulate the IF signal for display of the television information.

The tuner module 108 comprises a downconverter 202, the PLL 112, an address decoder 210, a memory unit 203, and a digital-to-analog (D/A) converter 204. In response to user selection of the desired television channel, the microprocessor 102 communicates the tuning command via the communication bus 108 to the PLL 112. The PLL 112 couples the tuning command to the

address decoder 210. The address decoder 210 determines the address in the memory unit 203 where the alignment data for the desired television channel resides. The address decoder 210 retrieves the alignment data from the memory unit 203 and couples the data to the PLL 112. The PLL 112 causes the PLL oscillator 208 to retrieve suitable alignment data from memory to select the desired television channel from the plurality of channels in the received RF signal. The electronic alignment allows the other frequency sensitive circuits of the tuner to be modified.

The PLL 112 comprises a digital integrated circuit (IC) PLL. Therefore, the D/A converter 204 converts the digital alignment data retrieved from the memory to analog voltages to be input to the downconverter 202. The downconverter 202 heterodynes the RF signal received by the RF source 110 with the frequency tone generated by the PLL 112 to output an RF signal corresponding to the desired television channel. The downconverters frequency selective circuits and other circuits are aligned with the D/A converter voltage outputs. One system that provides such tracking is described in U.S. Patent No. 5,678,211, issued October 14, 1997 to D. Badger, entitled "TELEVISION TUNING APPARATUS" (Incorporated herein by Reference).

FIGs. 3 and 4 show two exemplary block diagram embodiments of a PLL integrated circuit 207 that are most preferably contained in the tuner 108, that most preferably comprises an integrated circuit. In each one of the embodiments, the PLL nonvolatile memory 203, internal to a PLL integrated circuit, is implemented to store the alignment data for each Digital to Analog Converter (DAC).

The PLL integrated circuit includes a DAC section 301a, a communication bus section 301b, and a PLL section 301c. The communication bus section includes a shift register 303 and a communication bus receiver 302 that connects to the communication bus 106 (shown in FIG. 1). The PLL section 301c comprises a latch 330, a PLL programmable divider 302, and an address decoder 334. The DAC section comprises a plurality of DAC components 306a, 306b, and 306c, the PLL nonvolatile memory 203, a plurality of latches 312a to 312d, an communication decoder 308, and a shift register 310.

Each DAC component 306a, 306b, and 306c includes a respective converter 318a, 318b, 318c, a respective amplifier 320a, 320b, and 320c, and a respective input. Though three DAC components 306a, 306b, and 306c are shown, as many DAC converters as may be utilized to comply with the memory requirements are used.

A PLL frequency tuning command that is sent to the PLL module 207 via the communication bus 106 will be decoded to address a memory location in the PLL nonvolatile memory 203 that corresponds to the stored alignment data. The alignment data is then retrieved from the PLL nonvolatile memory 203. The retrieved alignment data is sent to the corresponding DAC, whose output is amplified by the respective amplifier 320a, 320b, or 320c to produce an alignment voltage. Such an alignment voltage is automatically retrieved whenever the microprocessor commands the tuner to tune a particular RF channel.

The frequency of PLL circuit operation is set in part by the PLL Programmable Divider 332. An exemplary frequency division ratio (N) is given by an equation such as:

$$N = 16384XN_{14} + 8192XN_{13} + \ldots + 4XN_2 + 2X\,N_1 + N_0$$

The address decoder 334 is a logic circuit that is programmed to divide the selected frequency range of the PLL circuit for the application into a number of alignment ranges. These alignment ranges need not be equal in frequency span. The highest-resolution alignment occurs when each frequency to be tuned is assigned an address where alignment data will be stored.

The address decoder 334 takes the digital frequency programming information sent to PLL programmable divider 332 and creates addresses that are used to access PLL nonvolatile memory locations. The logic of the address decoder is designed to access alignment data for a plurality of frequency channels that can be tuned, or can be designed to access alignment information for each channel tuned. The address decoder can be configured in software, e.g. a microprocessor running a software program, or alternatively in hardware, e.g. a series of logic gates arranged to provide the logic behind the address decoder. There are a wide variety of possible digital or analog configurations that are possible for the address decoder. However, it several exemplary embodiments are provided.

The address decoder 334 takes the digital frequency word commanded through the communication bus, and generates an address control word that is used to access alignment data in the PLL nonvolatile memory that is in-turn provided to the D/A circuits.

Many different embodiments of address decoder 334 may be applied to the tuner 108. The address decoder, for example, may utilize a software program or alternatively may utilize a set of logic gates. FIG. 5 shows one embodiment of address decoder method 500 that is performed by software. The contants used in this example are for an NTSC tuner system that starts tuning

channel #2 (having a 101MHz LO frequency), uses a 62.5 kHz PLL step size, and uses three D/A converter circuits for electronic alignment.

The method 5000 starts with block 5002 in which the microprocessor sends a PLL divider ratio to the PLL integrated circuit 112. The divider ratio is a digital word that sets the frequency of the tuner. The PLL divider ratio is stored in the PLL integrated circuit 112.

The method 5000 continues to block 5004 in which the channel divider ratio digital word is subtracted from the PLL divider ratio digital word to derive the commanded tuning frequency. This constant, for example, is 065H (Hexadecimal) for channel #2 LO frequency of 101 MHz and a 62.6 PLL step size.

The method 5000 continues to block 5006 in which the bits of the commanded tuning frequency derived in block 5004 are shifted to the right by 5 bits to effect division by 16. In block 5008 the results of block 5006 are shifted to the left by two bits to effect multiplication by 4. The least significant 5 bits are shifted out and are not recovered, leaving the lowest three bits of the digital word cleared. This clearing reduces the magnitude of the number, and leaves room to increment the address to access the three D/A converter circuits.

The method 500 continues to block 5010 in which the initial value of N is set to 1. The purpose of N is to derive a set number that the method 5000 loops through blocks 5014, 5016, 5016, and 5018, e.g. three. In block 5012, the nonvolatile memory is accessed that contains the alignment data having the address derived in block 5008. In block 5014, the digital word that is output by the nonvolatile memory 203 in response to the memory access in block 5012 is latched into the D/A converter at the location corresponding to N=1.

The address word N is incremented by 1 in block 5016. Therefore, the second time that the loop containing blocks 5012, 5014, 5016, and 5016 are run, the value of N equals 2. The third time, N=3. Following decision block 5018, provided that N is less than 4, the method 500 continues to block 5012. The decision block 5018 continues within this loop formed by blocks 5012, 1014, 5016, and 5016 until N equals 4. Following decision block 5018 when N=4, the method 500 terminates.

Another embodiment of address generator is provided in U.S. Patent No. 5,724,546 that issued April 21, 1998 to Devin, entitled "METHOD AND DEVICE FOR ADDRESS DECODING IN AN INTEGRATED CIRCUIT MEMEORY" (Incorporated herein by Reference).

There are two embodiments of addressing schemes that may be performed by the address decoder, regardless of the configuration of the address

decoder. Any type of known addressing scheme may be utilized while remaining within the scope of the address decoder. The first addressing scheme is a 1 to 1 addressing scheme, in which each actual channel to be used corresponds to a discrete alignment channel. For example, if there are envisioned to be 181 actual channels (i.e. cable channels + VHF channels + UHF channels) that a particular tuner for a television system can tune, then a 1 to 1 addressing scheme requires the address decoder can individually address 181 alignment channels.

Another type of addressing scheme by the address decoder involves the use of fewer alignment channels than the number of actual channels. The address decoder uses an interpolation process to obtain the actual channels in response to the alignment channels. For example, assume that there are 29 alignment channels that can be used to derive the actual channels. A plurality, e.g. five, of actual channels may have frequencies that are contained between one adjacent pair of alignment channels. One actual channel may be aligned at twenty percent of the difference from the lower alignment channel to the higher alignment channel. The next actual channel is aligned at forty percent of the distance from the lower alignment channel to the upper alignment channel, etc. When the first channel is selected, the address decoder performs a piece-wise linear interpolation of twenty percent above the lower alignment channel to the adjacent alignment channel.

There are certain nonlinearities between adjacent alignment channels. For example, the distance between alignment channels at one end of the alignment channel spectra may not match the distance between alignment channels at another end of the alignment channel spectra. Therefore, the address decoder may adjust the interpolation process so the more actual channels are interspersed between adjacent ones of the alignment channels at the more sparse frequencies that at the more dense frequencies.

The PLL nonvolatile memory 203 can be programmed/ reprogrammed by transferring the data via the communication bus and stores it in the latch circuits on chip. Alternatively, the data transmitted over the communication bus may be stored directly onto the PLL nonvolatile memory 203 without the use of latches. The communication decoder 308 will be configured according to command received from the communication bus receiver, to send the Write command to the appropriate PLL nonvolatile memory 203 so that the data can be stored.

The elements the PLL Section 301c operates as part of a larger PLL loop. The elements within the DAC section 301a operate for the electronic alignment function. The communication bus receiver block 302 is common to both.

In FIG. 3, a plurality of PLL nonvolatile memorys 203a, 203b, 203c, and 203d, internal to an PLL integrated circuit, are associated with respective D/A converters 318a, 318b, or 318c and the Reference Voltage circuit 316. This multiple PLL nonvolatile memory configuration results in the use of multiple, individual PLL nonvolatile memories 203a, 203b, and 203c. In FIG. 4, a single, larger PLL nonvolatile memory 203 is used. A more complex address algorithm is used in the FIG. 4 embodiment of one PLL nonvolatile memory.

Although a PLL nonvolatile memory is the memory circuit described in the PLL nonvolatile memory 203, 203a, 203b, 203c, and 203d, any type of known non-volatile re-writable memory circuit that can be positioned on a PLL integrated circuit for storing tuning alignment data is within the scope of the term PLL nonvolatile memory.

The communication bus receiver 302 includes an interface between the communication bus 106. The interface is controlled by the microprocessor 102 on the chassis 154 and the circuitry of the PLL element 112. The communication bus receiver 302 generates data, clock timing, and control signals for use within a PLL integrated circuit 203. The communication bus receiver 302 can be operated bi-directionally. That is, signals taken from the PLL element 112 can also be formatted, and transmitted over the communication bus for external use.

Shift register 303 formats the serial data taken from the communication Bus Receiver 302 into a parallel data word that determines the PLL frequency to which the PLL element 112 will be tuned. The PLL frequency relates to the channel selected, the countries that the tuner is used in, and other such factors. Latch 330 holds the digital word that determines PLL frequency. The hold timing of the latch 330 is controlled by a signal from the communication bus receiver.

The PLL programmable divider 332 uses the digital frequency control word to set a divide ratio that determines the frequency of operation of the PLL, and determines the frequency to be tuned in response to the input from the PLL circuit.

The shift register 310 takes the serial data from the communication bus receiver 302 and formats it into a parallel data word that is used to write alignment data into the PLL nonvolatile memory 203.

Latches 312a to 312d hold the digital word for electronic alignment to be written into the PLL nonvolatile memory 223. The latches 312a to 312d are not necessary if the PLL nonvolatile memory 223 interfaces directly with the shift register 310.

The communication decoder 308 takes commands sent through the communication decoder and generates control signals. One set of signals controls the timing for latches 312a to 312d, to store alignment data. A second set of signals commands the PLL nonvolatile memory 203 to receive and store data.

PLL nonvolatile memory 203 stores digital alignment information words in an addressable format. The correct alignment digital word is accessed according to the address from the address decoder 334, and is sent to the converters 318a to 318c. Stored information may also include D/A voltage step-size information, the commanded output voltage, and other information used by the D/A circuit to set the output voltage.

D/A converters 318a to 318c take the digital words recalled from the PLL nonvolatile memory 203 and translates them into an analog voltages that are used to control tuner alignments and other functions in the tuner. Amplifiers 320a to 320c amplify the analog voltages output by the respective D/A converters 318a to 318c to a range of voltages suitable to control tuner circuits. Input tuning voltage VTUN, generated by another area of the PLL circuit (not shown) in a usual manner, is summed into the output voltages, of the D/A converters 318a to 318c.

Reference voltage indicates circuit that generates a precise voltage for use by the D/A and other circuits within the PLL element 112. This voltage can be aligned similarly to the D/A circuits 306 if desired.

The alignment data in above embodiments is contained in nonvolatile memory stored in the tuner 108. As such, when a tuner module is transported, the alignment data is transported therein. The installation of the tuner containing the alignment data obviates further alignment data input instead of the alignment data having to be programmed into a distinct circuit component follower assembly of the components in the television receiver. If a tuner is malfunctioning, a new tuner having its alignment data is inserted into the malfunctioning television receiver. Once again, the repair person does not have to program separate alignment data into the nonvolatile memory 104 such as, for example, a chassis EEPROM.

Although various embodiments that incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.